



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 09/425,401 Confirmation No.: 9510
Applicant: John S. Yates, Jr., et al.
Title: PROFILING PROGRAM EXECUTION TO IDENTIFY FREQUENTLY
EXECUTED PORTIONS AND ASSIST BINARY TRANSLATION
Filed: October 22, 1999
Art Unit: 2124
Examiner: John Q. Chavis

Atty. Docket: 114596-09-4016
Customer No. 38492

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

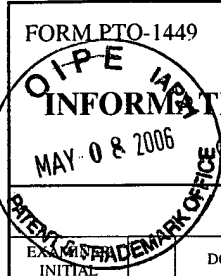
In accordance with 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant wishes to make of record the items listed on the accompanying Form PTO-1449. Applicant respectfully requests the Examiner to fully consider the items and independently ascertain their teaching before issuance of the next action, and to make them of record in the file. The Examiner is also requested to initial and return a copy of the enclosed Form PTO-1449 to evidence such consideration.

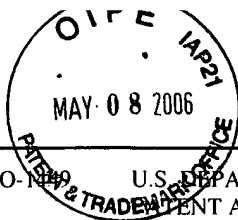
1. Applicant has listed publication dates on the attached Form PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated. Applicant reserves the right to establish the patentability of the claims over any information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

2. The references listed on the enclosed Form 1449 are references that have come to light in applications listed in the Information Disclosure Statement of February 2002. For many of the listed

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I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on May 5, 2006 as First Class Mail in an envelope with sufficient postage addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

FORM PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 114596-09-4016		SERIAL NO. 09/425,401	
		INFORMATION DISCLOSURE CITATION					
		(Use several sheets if necessary)					
		APPLICANT John S. Yates, Jr., et al.		FILING DATE October 22, 1999		GROUP ART UNIT 2124	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	4,077,058	2/28/1978	Appell	717	162	Dec. 2, 1974	
	4,275,441	06/23/1981	Takeuchi	714	38	Mar. 27, 1979	
	4,722,050	01/26/1988	Lee	712	205	Mar. 27, 1986	
	4,831,515	05/16/1989	Kamada	712	207	Feb. 10, 1986	
	5,121,472	06/09/1992	Danish	710	67	May 31, 1989	
	5,371,894	12/06/1994	DiBrino	714	34	Dec. 23, 1993	
	5,377,309	12/27/1994	Sonobe	706	60	Nov. 27, 1991	
	5,404,473	04/04/1995	Papworth	712	241	Mar. 1, 1994	
	5,675,332	10/07/1997	Limberg	341	67	Oct. 7, 1997	
	5,721,855	02/24/1998	Hinton	712	218	Jul. 12, 1996	
	5,729,728	03/17/1998	Colwell	712	234	Sep. 6, 1996	
	5,918,251	06/29/1999	Yamada	711	207	Dec. 23, 1996	
	5,926,484	07/20/1999	Takusagawa	714	710	Oct. 28, 1996	
	6,035,120	03/07/2000	Ravichandran	717	141	May 28, 1997	
	6,065,103	05/16/2000	Tran	711	156	Dec. 16, 1997	
	6,088,793	07/11/2000	Liu	712	239	Dec. 30, 1996	
	6,128,641	10/03/2000	Fleck	718	108	Sep. 12, 1997	
	6,157,993	12/5/2000	Lewchuk	711	213	Jan. 3, 2000	
	6,199,095	3/6/2001	Robinson	709	107	Jan. 29, 1996	
	6,249,862	06/19/2001	Chinnakonda	712	218	Nov. 15, 2000	
	6,256,775	7/3/2001	Flynn	717	127	Dec. 11, 1997	
	6,351,646	02/26/2002	Jellema	455	461	Apr. 20, 1998	
	6,415,379	07/02/2002	Keppel	712	209	Oct. 13, 1999	
	6,418,460	07/09/2002	Bitar	718	108	Feb. 18, 1997	
	6,535,903	3/18/2003	Yates	718	100	Jan. 29, 1996	
	6,549,959	04/15/2003	Yates	710	22	Nov. 4, 1999	
	6,553,431	04/22/2003	Yamamoto	710	8	Jul. 21, 1999	
	6,564,339	05/13/2003	Swoboda	714	30	Jan. 14, 2000	
	6,591,340	07/08/2003	Chopra	711	118	Jun. 10, 2002	
	6,685,090	02/03/2004	Nishigaya	235	382	Jan. 26, 2001	
	6,694,457	02/17/2004	McKee	714	38	Mar. 6, 2001	
	6,708,173	03/16/2004	Behr	707	10	Oct. 18, 2000	
EXAMINER			DATE CONSIDERED				



FORM PTO-1049 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)				ATTORNEY DOCKET NO. 114596-09-4016		SERIAL NO. 09/425,401	
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,721,941	4/13/2004	Morshed	717	127	Aug. 22, 2000
		6,763,452	07/13/2004	Hohensee	712	227	Jun. 24, 1999
		6,779,107	08/17/2004	Yates	712	229	Oct. 28, 1999
		6,789,181	09/07/2004	Yates	712	4	Nov. 3, 1999
		6,789,263	09/07/2004	Shimada	725	119	Jun. 18, 1997
		6,820,051	11/16/2004	Swoboda	703	28	Jan. 14, 2000
		6,820,190	11/16/2004	Knebel	712	215	Feb. 2, 2000
		6,826,748	11/30/2004	Hohensee	717	130	Jun. 24, 1999
		6,934,832	08/23/2005	Van Dyke	712	244	Sep. 21, 2000
		6,941,545	09/06/2005	Reese	717	130	May 28, 1999
		6,954,923	10/11/2005	Yates	717	130	Jul. 7, 1999
		6,978,462	12/20/2005	Adler	719	318	Jun. 11, 1999
		7,013,456	03/14/2006	Van Dyke	717	130	Jun. 16, 1999
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Papers, Etc.)							
		Dean, ProfileMe: Hardware Support for Instruction-Level Profiling on Out-of-Order Processors," Proceedings of 30th Annual Intl. IEEE/ACM Symp. on Microarchitecture, pp. 292-302 (Dec. 1997)					
		Hollingsworth, Critical Path Profiling of Message Passing and Shared-Memory Programs, IEEE Transactions on Parallel and Distributed Systems vol. 9, no. 10, pp. 1029-1040 (October 1998)					
		Intel Corporation, Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, pages 3-10 to 3-13, 7-1 to 7-3, 7-20 to 7-25; Volume 2: Instruction Set Reference, pages 3-60 to 3-63, 3-240 to 3-251; Volume 3: System Programming Guide, pages 11-1 to 11-3, 11-10 to 11-13, 14-1 to 14-3, 14-10 to 14-15 (1997)					
		Intel Corporation, Pentium Processor Family Developer's Manual (1997), pages 1-1 to 1-6, 2-1 to 2-20					
		Intel Corporation, Pentium Processor Family Developer's Manual (1997), vol. 3: Architecture and Programming Manual, pages 3-1 to 3-3, 3-10 to 3-13, 12-1 to 12-27, 14-1 to 14-30					
		Jones, Puzzling with Microcode, ACM SIGARCH Computer Architecture News, vol. 11, no. 5, pp. 8-12 (1983)					
		Magnusson and Werner, Efficient Memory Simulation in SimICS, Proceedings of the 28th Annual Simulation Symposium, IEEE, pp. 62-73 (1995).					
EXAMINER				DATE CONSIDERED			

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